Outline for Today's Lecture

- Binary Arithmetic
- Two’s Complement
- Logic Levels
- CMOS Transistors
- Intro Logic Circuits
Addition

• Decimal

3734
+ 5168
_____  
10110

• Binary

1011
+ 0011
_____  
00111
Addition

- Decimal

\[
\begin{array}{c}
3734 \\
+ 5168 \\
\hline
8902
\end{array}
\]

\[11 \text{ carries}\]

- Binary

\[
\begin{array}{c}
1011 \\
+ 0011 \\
\hline
1110
\end{array}
\]

\[11 \text{ carries}\]
Binary Addition Examples

• Add the following 4-bit binary numbers

\[
\begin{array}{c}
1001 \\
+ \ 0101 \\
\hline
1010
\end{array}
\]

• Add the following 4-bit binary numbers

\[
\begin{array}{c}
1011 \\
+ \ 0110 \\
\hline
1101
\end{array}
\]
Binary Addition Examples

• Add the following 4-bit binary numbers

\[
\begin{array}{c}
1001 \\
+ 0101 \\
\hline
1110
\end{array}
\]

• Add the following 4-bit binary numbers

\[
\begin{array}{c}
111 \\
+ 1011 \\
+ 0110 \\
\hline
10001
\end{array}
\]

Overflow!
Overflow

• Digital systems operate on a **fixed number of bits**
• Overflow: when result is too big to fit in the available number of bits
• See previous example of $11 + 6$
Signed Binary Numbers

- Sign/Magnitude Numbers
- Two’s Complement Numbers
Sign/Magnitude Numbers

• 1 sign bit, N-1 magnitude bits

• Sign bit is the most significant (left-most) bit
  – Positive number: sign bit = 0
  – Negative number: sign bit = 1

• Example, 4-bit sign/mag representations of ±6:
  +6 =
  -6 =

• Range of an N-bit sign/magnitude number:
Sign/Magnitude Numbers

• 1 sign bit, $N$-1 magnitude bits
  • Sign bit is the most significant (left-most) bit
    – Positive number: sign bit = 0
    – Negative number: sign bit = 1

  • Example, 4-bit sign/mag representations of ±6:
    +6 = 0110
    -6 = 1110

  • Range of an $N$-bit sign/magnitude number:
    $$[-(2^{N-1}-1), 2^{N-1}-1]$$
Sign/Magnitude Numbers

• Problems:
  – Addition doesn’t work, for example -6 + 6:

\[
\begin{array}{c}
1110 \\
+ 0110 \\
\hline
10100 (\text{wrong!})
\end{array}
\]

  – Two representations of 0 (± 0):

\[
\begin{array}{c}
1000 \\
0000
\end{array}
\]
Two’s Complement Numbers

• Don’t have same problems as sign/magnitude numbers:
  – Addition works
  – Single representation for 0
Two’s Complement Numbers

- Msb has value of $-2^{N-1}$

$$A = a_{n-1} (-2^{n-1}) + \sum_{i=0}^{n-2} a_i 2^i$$

- Most positive 4-bit number:
- Most negative 4-bit number:
- The most significant bit still indicates the sign ($1 = \text{negative}, 0 = \text{positive}$)
- Range of an $N$-bit two’s comp number:
• Msb has value of $-2^{N-1}$

$$A = a_{n-1}(-2^{n-1}) + \sum_{i=0}^{n-2} a_i 2^i$$

• Most positive 4-bit number: 0111 (+7)
• Most negative 4-bit number: 1000 (-8)
• The most significant bit still indicates the sign (1 = negative, 0 = positive)
• Range of an $N$-bit two’s comp number: $[-(2^{N-1}), 2^{N-1}-1]$
# Number System Comparison

<table>
<thead>
<tr>
<th>Number System</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unsigned</td>
<td>[0, (2^N-1)]</td>
</tr>
<tr>
<td>Sign/Magnitude</td>
<td>[(-(2^{N-1}-1), 2^{N-1}-1)]</td>
</tr>
<tr>
<td>Two’s Complement</td>
<td>[(-2^{N-1}, 2^{N-1}-1)]</td>
</tr>
</tbody>
</table>

For example, 4-bit representation:

- **Unsigned**: 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1100 1101
- **Two’s Complement**: 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1100 1101
- **Sign/Magnitude**: 1111 1110 1111 1111 0010 0010 0010 0010 0000 0000 0000 0000 0000 0000 0000 0000

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“Taking the Two’s Complement”

• Flip the sign of a two’s complement number
• Method:
  1. Invert the bits
  2. Add 1
• Example: Flip the sign of $3_{10} = 0011_2$
“Taking the Two’s Complement”

- Flip the sign of a two’s complement number

**Method:**
1. Invert the bits
2. Add 1

**Example:** Flip the sign of $3_{10} = 0011_2$
1. $1100$
2. $+ 1$

\[
\begin{align*}
1101 & = -3_{10}
\end{align*}
\]

*Alternative Two’s Complement Method*: starting with the LSB write the same digits until you reach the first 1, keep the 1 and invert all other bits to its left
Two’s Complement Examples

- Take the two’s complement of $6_{10} = 0110_2$

- What is the decimal value of $1001_2$?
Two’s Complement Examples

• Take the two’s complement of $6_{10} = 0110_2$

  1. $1001$
  2. $+ 1$

  $\begin{align*}
  1010_2 &= -6_{10}
  \end{align*}$

• What is the decimal value of the two’s complement number $1001_2$?

  1. $0110$
  2. $+ 1$

  $\begin{align*}
  0111_2 &= 7_{10}, \text{ so } 1001_2 &= -7_{10}
  \end{align*}$
• Add 6 + (-6) using two’s complement numbers

\[
\begin{array}{c}
0110 \\
+ 1010 \\
\hline
\end{array}
\]

• Add -2 + 3 using two’s complement numbers

\[
\begin{array}{c}
1110 \\
+ 0011 \\
\hline
\end{array}
\]
• Add 6 + (-6) using two’s complement numbers

\[
\begin{array}{c}
111 \\
0110 \\
+ 1010 \\
\hline
10000
\end{array}
\]

• Add -2 + 3 using two’s complement numbers

\[
\begin{array}{c}
111 \\
1110 \\
+ 0011 \\
\hline
10001
\end{array}
\]
Logic Levels

• Discrete voltages represent 1 and 0
• For example:
  
  \[ 0 = \text{ground (GND)} \text{ or } 0 \text{ volts} \]
  
  \[ 1 = V_{CC} \text{ or } 5 \text{ volts} \quad [\text{TTL: } V_{CC} \quad \text{CMOS: } V_{DD}] \]

• What about 4.99 volts? Is that a 0 or a 1?
• What about 3.2 volts?
Logic Levels

• *Range* of voltages for 1 and 0
• Different ranges for inputs and outputs to allow for *noise*
What is Noise?

• Anything that degrades the signal
  – E.g., resistance, power supply noise, coupling to neighboring wires, etc.

• Example: a gate (driver) outputs 5 V but, because of resistance in a long wire, receiver gets 4.5 V
The Static Discipline

• With logically valid inputs, every circuit element must produce logically valid outputs

• Use limited ranges of voltages to represent discrete values
Logic Levels
Noise Margins

Driver

Receiver

Output Characteristics

Input Characteristics

Logic High Output Range

Logic Low Output Range

GND

$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$
DC Transfer Characteristics

Ideal Buffer:

Real Buffer:

\[ V_{OH} = V_{DD} \]

\[ V_{OL} = 0 \]

\[ V_{DD} / 2 \]

\[ V_{IL}, V_{IH} \]

Unity Gain Points
Slope = 1

\[ NM_H = NM_L = V_{DD} / 2 \]

\[ NM_H, NM_L < V_{DD} / 2 \]
DC Transfer Characteristics

\[ V(A) \]

\[ V(Y) \]

Output Characteristics

Input Characteristics

Unity Gain Points
Slope = 1

Forbidden Zone

\[ V_{OH} \]

\[ V_{OL} \]

\[ V_{DD} \]

\[ V_{IL} \]

\[ V_{IH} \]

\[ V_{DD} \]

\[ V_{IL} \]

\[ V_{IH} \]

\[ NM_H \]

\[ NM_L \]

\[ GND \]
## Logic Family Examples

<table>
<thead>
<tr>
<th>Logic Family</th>
<th>$V_{CC}$ or $V_{DD}$</th>
<th>$V_{IL}$</th>
<th>$V_{IH}$</th>
<th>$V_{OL}$</th>
<th>$V_{OH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTL</td>
<td>5 (4.75 - 5.25)</td>
<td>0.8</td>
<td>2.0</td>
<td>0.4</td>
<td>2.4</td>
</tr>
<tr>
<td>CMOS</td>
<td>5 (4.5 - 6)</td>
<td>1.35</td>
<td>3.15</td>
<td>0.33</td>
<td>3.84</td>
</tr>
<tr>
<td>LVTTL</td>
<td>3.3 (3 - 3.6)</td>
<td>0.8</td>
<td>2.0</td>
<td>0.4</td>
<td>2.4</td>
</tr>
<tr>
<td>LVCMOS</td>
<td>3.3 (3 - 3.6)</td>
<td>0.9</td>
<td>1.8</td>
<td>0.36</td>
<td>2.7</td>
</tr>
</tbody>
</table>
Transistors

- Logic gates built from transistors
- 3-port voltage-controlled switch
  - 2 ports connected depending on voltage of 3rd
  - d and s are connected (ON) when g is 1
Silicon

- Transistors built from silicon, a semiconductor
- Pure silicon is a poor conductor (no free charges)
- Doped silicon is a good conductor (free charges)
  - n-type (free negative charges, electrons)
  - p-type (free positive charges, holes)
MOS Transistors

• Metal oxide silicon (MOS) transistors:
  – Polysilicon (used to be metal) gate
  – Oxide (silicon dioxide) insulator
  – Doped silicon
Transistors: nMOS

**Gate = 0**

OFF (no connection between source and drain)

**Gate = 1**

ON (channel between source and drain)
Transistors: pMOS

• pMOS transistor is opposite
  – ON when Gate = 0
  – OFF when Gate = 1
Transistor Function

\[ g = 0 \quad nMOS \quad \text{OFF} \]
\[ g = 1 \quad pMOS \quad \text{ON} \]

\[ g = 0 \quad nMOS \quad \text{OFF} \]
\[ g = 1 \quad pMOS \quad \text{ON} \]
Transistor Function

• **nMOS**: pass good 0’s, so connect source to GND

• **pMOS**: pass good 1’s, so connect source to $V_{DD}$
CMOS Gates: NOT Gate

\[ Y = \overline{A} \]

<table>
<thead>
<tr>
<th>A</th>
<th>P1</th>
<th>N1</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
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CMOS Gates: NOT Gate

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<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>1</td>
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<tr>
<td>1</td>
<td>OFF</td>
<td>ON</td>
<td>0</td>
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CMOS Gates: NAND Gate

NAND

\[ Y = \overline{AB} \]

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<tr>
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<tr>
<td>0</td>
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CMOS Gates: NAND Gate

\[ Y = AB \]

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<tbody>
<tr>
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CMOS Gates: NAND Gate

NAND

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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>ON</td>
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<td>0</td>
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CMOS Gate Structure

- **Inputs**
- **pMOS Pull-up Network**
- **nMOS Pull-down Network**
- **Output**
NOR Gate

How do you build a three-input NOR gate?
NOR3 Gate
A logic circuit is composed of:

- Inputs
- Outputs
- Functional specification
- Timing specification
Circuits

• Nodes
  – Inputs: A, B, C
  – Outputs: Y, Z
  – Internal: n1

• Circuit elements
  – E1, E2, E3
  – Each a circuit
Types of Logic Circuits

• **Combinational Logic**
  – Memoryless
  – Outputs determined by current values of inputs

• **Sequential Logic**
  – Has memory
  – Outputs determined by previous and current values of inputs

![Diagram](functional spec)