Outline for Today's Lecture

• Programmable Logic Devices
  – PLA
  – PAL
  – CPLD
  – FPGA
  – SoC
Programmable Logic Devices (PLD)

- PLDs are chips that contain programmable circuits
  - Contain a large number of digital gates that can be programmed
  - Offer more flexibility and scale than the discrete 7400 series TTL chips used in our initial lab
  - PLA (Programmable Logic Array) and PAL (Programmable Array Logic) are PLDs which have planes of AND and OR gates interconnected to each other and which could be programmed
PLAs

- Plane of AND gates and OR gates to express any function as a sum of product of minterms
- \( X = \overline{A}\overline{B}C + AB\overline{C} \)
- \( Y = A\overline{B} \)
PLAs: Implementation

- Reprogrammable connections provide flexibility of realizing digital circuits
PLAs: Dot Notation

- $X = \overline{A}BC + ABC$
- $Y = AB$
PALs

- A PAL difference from a PLA in that the OR gate plane is fixed while the AND plane is programmable

Example: 22V10 PAL
- More flexible than 7400 series TTL
- Up to 22 inputs and 10 outputs
- $2 \times (6 \text{ thought } 16)$ product terms
Difference of PLA and PALs

- PLA has both programmable AND and OR planes whereas PAL has only programmable AND planes and OR plane is fixed.
- PLA has more flexibility in the logic circuit function implementation than PAL.
- PAL is simpler to manufacture than PLA.
- PLA have reduced speed performance.
- PAL devices are manufactured in smaller size.
Complex PLD (CPLD)

- CPLDs offer larger number of gates and I/O pins than PLAs or PALs
- CPLD are designed with reprogrammable non-volatile EEPROM to maintain configuration after re-boot
- CPLDs provide 100’s to 1000’s of gates compared to 10’s gates in PLA or PAL

Altera MAX 7000-series CPLD with 2500 gates
FPGA: Field Programmable Gate Array

- FPGAs provide 100K’s of gates to support larger designs
- Include additional digital building blocks (eg flip-flops, memory arrays, multipliers, transceivers,…) for more complex applications
FPGA: Field Programmable Gate Array

• Composed of:
  – **LEs** (Logic elements): perform logic
  – **IOEs** (Input/output elements): interface with outside world
  – **Programmable interconnection**: connect LEs and IOEs
  – Some FPGAs include other building blocks such as multipliers and RAMs
General FPGA Layout
LE: Logic Element

• Composed of:
  – **LUTs** (lookup tables): perform combinational logic
  – **Flip-flops**: perform sequential logic
  – **Multiplexers**: connect LUTs and flip-flops
Altera Cyclone IV LE

• The Altera Cyclone IV has up to 150 LEs
• Each LE has:
  – 1 four-input LUT
  – 1 registered output
  – 1 combinational output
Altera Cyclone IV LE
Show how to configure a Cyclone IV LE to perform the following functions:

- $X = \overline{ABC} + ABC$
- $Y = AB$
Show how to configure a Cyclone IV LE to perform the following functions:

- \( X = \overline{ABC} + ABC \)
- \( Y = A\overline{B} \)

### LE Configuration Example

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SoC: System On a Chip

• SoCs had embedded microprocessing and DSP functionality to FPGA LEs in an integrated chip

• Example Altera Arria® 10 SoC includes
  • 1.5GHz dual core ARM A9, hardened floating point DSP blocks, DDR4 SDRAM, PCIe blocks, up to 660K LEs and 3K multipliers

• Example Altera Stratix® 10 SoC includes
  • 1.5GHz quad core ARM Cortex A53, PCIe blocks, Ethernet blocks, hi-speed Xcvrs, 3K DSP blocks, up to 2M Les and 6K multipliers
PLD Design Flow

Using a CAD tool (such as Altera’s Quartus II)

• **Enter the design** using schematic entry or an HDL

• **Simulate** the design

• **Synthesize** design and map it onto PLD

• **Download the configuration** onto the PLD

• **Test** the design